#11/Amdt
1.7.0328
C. Moore

ATTENTION: BOX AFTER FINAL
RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE REQUESTED
EXAMINING GROUP 2814

PATENT
Customer No. 22,852
Attorney Docket No. 04329.2613

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Katsuhiko HIEDA	)	Group Art Unit: T. Le
	)	
Application No.: 09/916,509	)	Examiner: 2814
	)	
Filed: July 30, 2001	)	
	)	
For: FIELD EFFECT TRANSISTOR USING SIDE-WALL GATES TO PREVENT PUNCH-THROUGH (As Amended)	)	

Commissioner for Patents
Washington, DC 20231

Sir:

Please
DO NOT Enter
T.L.
01/08/02

AMENDMENT AFTER FINAL

In reply to the Final Office Action dated October 24, 2002, the period for response to which extends through January 24, 2003, please amend the application as follows:

IN THE CLAIMS:

Please amend claims 1 and 2 as follows:

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

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Washington, DC 20005
202.408.4000
Fax 202.408.4400
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1. (Twice Amended) A semiconductor device comprising:

a convex semiconductor layer provided on a semiconductor substrate;